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| EXAMINER | |
|---|---|
| XIAO, KE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2675 | |

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/644,151 | WATERMAN, JOHN KARL | |
| | Examiner | Art Unit | |
| | Ke Xiao | 2675 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

Claim 13 is objected to because of the following informalities:

Claim 13, line 1 recites the limitation "writing a line of aid" which the examiner suggests be changed to -- writing a line of an --.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claims 8, 10-16** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Claim 8** recites the limitations "RAM interface", "input FIFO", and "output FIFO" in lines 1-4. There is insufficient antecedent basis for this limitation in the claim. The examiner suggests that the claim be amended to be dependent upon claim 3 instead of claim 1 in order to overcome this limitation. The claim will be examined as per suggested amendment.

**Claim 10** recites the limitation "the liquid crystal micro display" in line 10. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1-2, 10-12 and 15-16** are rejected under 35 U.S.C. 102(e) as being anticipated by Konno (US 2003/0080932).

Regarding **Claim 1**, Konno teaches a liquid crystal display system comprising:

a display driver integrated circuit (Konno, Fig. 7 element 107);

a memory coupled to the display driver integrated circuit (Konno, Fig. 7 elements 103A and 103B); and

at least one liquid crystal micro display coupled to the display driver integrated circuit (Konno, Fig. 7 elements 201-208) wherein a frame of video information is written to the memory in a same time period as a previously stored frame of video information is read from the memory more than one time and provided to the liquid crystal micro display (Konno, Figs. 1 and 8 first and second write periods). Specifically Konno teaches the use of an alternate buffer form which means that the buffers and alternately and simultaneously being read and write (Konno, Pg. 7 paragraph [0079-0080]).

Regarding **Claim 2**, Konno further teaches that the previously stored frame of video information is read from the memory two times to provide a non-inverted and

inverted frame of video information to prevent degradation of the liquid crystal micro display (Konno, Figs. 1 and 4 negative polarity and positive polarity).

Regarding **Claims 10 and 11**, Konno teaches a method of providing frames of video information to a liquid crystal display comprising repeating the steps of:

providing frames of video information (Konno, Fig. 7-8);

identifying a start of an incoming frame of video information (Konno, Fig. 8 start of FM1r and FM2r pulses);

writing the incoming frame of video information to a memory within a time period having a predetermined duration (Konno, Fig. 8 on period of FM1w and FM2w);

reading a previously stored frame of video information more than one time from the memory during the same time period (Konno, Fig. 8 element 603);

providing the previously stored frame of video information more than one time to a liquid crystal micro display (Konno, Figs. 1 and 8 element 603).

Regarding **Claim 12**, Konno further teach that memory write and read steps further include:

writing a line of the incoming frame of video information to the memory (Konno, Fig. 8, elements FM1w and 602);

reading more than one line of the previously storage frame of video information from the memory (Konno, Fig. 8 elements FM2r and 603); and

repeating the steps of writing a line and reading more than one line until the incoming frame is written to the memory and the previously store frame of video

information has been read out more than one time (Konno, Fig. 8 odd frame even frame repeat steps).

Regarding **Claim 15**, Konno further teaches the steps of:

partitioning the memory into a first area and a second area (Konno, Fig. 7 elements 103A and 103B);

storing the previously stored frame of video information in the first area of the memory (Konno, Fig. 8 after FM1w is off FM1r is on meaning after writing to first frame memory you then read from it); and

storing the incoming frame of video information in the second area of the memory wherein subsequent incoming frames of video information toggle back and for the being written into the first and second areas of the memory (Konno, Fig. 8 after incoming data is then stored to frame memory 2 during FM2w on period and the frame memories alternate in order to supply the display with video data).

Regarding **Claim 16**, Konno further teaches including a step of overwriting the previously stored frame of video information with video information of the incoming frame after the previously stored frame of video information has been read for a final time such that the memory requires less than two frames of storage capability (Konno, Fig. 12, there is only one frame memory compared to two frame memories of Pg. 10 paragraph [0111-00161] which means that an addressed memory write can only occur after the specific data has finished being read out in the case where one frame is the capacity of the frame memory).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 3-8, 13-14 and 17-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Konno (US 2003/0080932) in view of Hashimoto (US 4,882,710).

Regarding **Claim 3**, Konno fails to teach that the memory system includes input/output FIFOs and a RAM interface coupled to the FIFOs. Hashimoto teaches a memory system which includes FIFO input/output buffers (Hashimoto, Abstract);

a RAM interface unit coupled to the input FIFO and the memory (Hashimoto, Abstract, Fig. 1 elements Read Reset Controller); and

an output FIFO coupled to the RAM interface unit and the liquid crystal micro display (Hashimoto, Abstract).

It would have been obvious to replace the memory system of Konno with the memory system of Hashimoto in order to increase operating speed (Hashimoto, Col. 1 lines 32-39).

Regarding **Claim 4-7**, Hashimoto further teaches that the input/output FIFO buffers are capable of storing one or more lines of video information corresponding to the largest video format supported by the display driver integrated circuit. Overflow conditions are inherently prevented (Hashimoto, Abstract).

Regarding **Claim 8**, the combination of Konno and Hashimoto inherently teaches that the modified RAM interface of Hashimoto controls the input FIFO, memory, and the output FIFO such that the output FIFO has an output frame rate greater than an input frame rate to the input FIFO. The output FIFO will need to output at twice the speed in order for Konno's invention to operate correctly.

Regarding **Claim 13**, Konno fails to teach the use of FIFO during the step of writing a line to memory as claimed. Hashimoto further teach that the step of writing a line of video data further includes the steps of:

storing the line of the incoming frame of video in formation in a FIFO (Hashimoto, Abstract); and

writing the line storage in the FIFO to the memory (Hashimoto, Abstract).

It would have been obvious to replace the memory system of Konno with the memory system of Hashimoto in order to increase operating speed (Hashimoto, Col. 1 lines 32-39).

Regarding **Claim 14**, Konno teaches that the step of reading more than one line of the previously stored frame of video information from memory further includes the steps of:

reading a line from the previously storage frame of video information and the memory (Konno, Fig. 1 first writing period);

providing the video information to the liquid crystal micro display;

reading at least one more line from the previously storage frame of video information (Konno, Fig. 1 second writing period);

providing the at least one more line to the liquid crystal micro display.

Konno fails to teach the use of a FIFO in the step of reading as claimed. Hashimoto teaches the use of an output FIFO where the output from the frame memory is stored in the FIFO buffer and then output to the receiver (Hashimoto, Abstract). It would have been obvious to add the FIFO of Hashimoto to the memory device of Konno in order to increase the operating speed of the Konno's memory device.

Regarding **Claim 17**, Konno teaches a frame buffer section of a liquid crystal micro display driver integrated circuit for interfacing with a memory comprising (Konno, Fig. 7 elements 103A 103B and 107):

an input coupled for receiving incoming video information (Konno, Fig. 7 elements 101 and 112);

an output for providing video information to other circuitry of the liquid crystal micro display driver integrated circuit (Konno, Fig. 7 output switching); and

a RAM interface unit coupled to the input and output and the memory wherein the RAM interface unit manages writing stored video information in the input corresponding to an incoming frame of video information to the memory and manages reading stored video information from the memory corresponding to a previously stored frame of video information (Konno, Fig. 7 element 104 and 105) to the output such that a rate at which video information outputs the output is greater than a rate at which video information is input to the input (Konno, Fig. 7 and 8).

Konno fails to teach that the input and output are FIFOs. Hashimoto teaches a dynamic memory system with FIFO read/write buffers usable as a frame buffer which

reads and writes into memory at the same time (Hashimoto, Abstract). It would have been obvious to one of ordinary skill in the art to replace the memory system of Konno with the memory system including the input/out FIFOs of Hashimoto in order to increase the speed of operation.

Regarding **Claim 18**, Konno further teaches that the memory is capable of storing two frames of video information (Fig. 7 elements 103A and 103B).

Regarding **Claims 19 and 20**; Hashimoto further teaches that the input/output FIFOs are capable of storing one or more lines of video information (Hashimoto, Abstract two ore more lines).

Regarding **Claim 21**, Konno teaches a method of handling video information for a liquid crystal micro display comprising steps of:

writing video information into a memory (Konno, Fig. 7 input switching);

reading video information from a previously stored frame of video information in the memory (Konno, Fig. 7 output switching);

providing the video information that was read out from memory to a liquid crystal micro display (Konno, Fig. 7 element 107 output to the matrix); and

repeating the steps listed above such that the incoming frame is written to the memory and the previously stored frame of video information is read out at least once from the memory in a same time period (Konno Fig. 7 and 8 above steps are repeated for every frame).

Konno fails to teach the use of input/output FIFOs during the read and write steps as claimed. Hashimoto teaches a memory system for use as a frame buffer including:

storing video information from an incoming frame into an input FIFO;

writing video information stored in the input FIFO to a memory; and

reading video information from a previously storing frame of video information in the memory to an output FIFO (Hashimoto, Abstract).

It would have been obvious to replace the memory system of Konno with the memory system of Hashimoto in order to increase operating speed.

Regarding **Claim 22 and 23**, Hashimoto further teaches that the steps storing information from an incoming frame into an input FIFO further include storing one or more lines of video information to the input FIFO.

**Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Konno (US 2003/0080932) in view of Mitsui (US 5,729,313).

Regarding **Claim 9**, Konno fails to teach that each micro display comprises a first, second, and third crystal micro displays coupled to the display driver integrated circuit. Mitsui teaches that each micro display can be comprised of a first, second, and third reflective crystal micro displays. It would have been obvious to modify the liquid crystal display of Konno to be a reflective color display as taught by Mitsui with first (red), second (green), and third (blue) reflective crystal micro display in order to add the ability to display color and to conserve power.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571)272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 14th, 2005 - kx -

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